

1 17. (original) In a computer system having a source computer and a  
2 destination computer having a clock that regulates timing of activities at the destination  
3 computer, a method comprising the steps of:

4 providing a logical structure for encapsulating multiple streams of data, said  
5 streams of data being stored in packets;

6 storing clock licenses that dictate advancement of a clock in multiple ones of the  
7 packets;

8 transmitting the logical structure from the source computer to the destination  
9 computer; and

10 for each packet that holds a clock license, advancing the clock at the destination  
11 computer as dictated by the clock license in response to receiving the packet at the  
12 destination computer.

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15 18. (currently amended) The method of claim 4317 wherein each clock  
16 license includes a time value to which the clock at the destination computer is to be  
17 advanced.

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19 19. (original) The method of claim 18 wherein each clock license  
20 includes an expiration time after which the clock license is invalid.

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22 37. (previously amended) In a computer system, a computer-readable storage  
23 medium holding a logical structure that encapsulates components comprising:  
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25 multiple streams of data wherein the streams of data are stored in packets;

clock licenses that each dictate advancement of a clock that regulates rendering of the data in the packets.

38. (currently amended) The computer-readable storage medium of claim 5337 wherein each clock license includes a time value to which the clock at the destination computer is to be advanced.

39. (original) The computer-readable storage medium of claim 38 wherein each clock license includes an expiration time after which the clock license is invalid.

42. (previously amended) A data processing system comprising:

- a source computer with a storage;
- a logical structure stored in storage for encapsulating multiple data streams, data from said data streams being incorporated in packets;
- a clock license being encapsulated into at least one packet for advancing a clock at a destination when processed at the destination.

43. (currently amended) In a computer system having a source computer and a destination computer having a clock that regulates timing of activities at the destination computer, a ~~The method as defined in Claim 17, wherein:~~ comprising the steps of: providing a logical structure for encapsulating multiple streams of data, said streams of data being stored in packets, comprises: by:

storing samples of data from multiple data streams in the packets;

storing replicas of information in at least some of the packets;

storing error correcting data in the at least some of the packets, wherein the error correcting data identifies an error correcting method for the at least some of the packets;

setting a flag in the packets that hold the replicas; and

encapsulating the packets into the logical structure, wherein at least some of the packets hold the replicas;

storing clock licenses that dictate advancement of a clock in multiple ones of the

transmitting the packets of the logical structure on a packet-by-packet basis over a

switched network from the source computer to the destination computer; and

for each packet that holds a clock license, advancing the clock at the destination

computer as dictated by the clock license in response to receiving the packet at the

destination computer, wherein the method further comprises transmitting the packets of

the logical structure on a packet-by-packet basis over a packet-switched network from the

source computer to the destination computer.

44. (previously added) The method as defined in Claim 43, wherein the replicas of information hold property information regarding the samples of data.

1           45. (previously added) The method of claim 43 wherein portions of a  
2 sample are stored in selected packets and a replica of property information regarding the  
3 sample is stored in each packet in which a portion of the sample is stored.

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5           46. (previously added) The method of claim 43, further comprising the step  
6 of examining one of the replicas of information at the destination computer when one of  
7 the packets is lost during the transmitting.

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10          47. (previously added) The method of claim 43, further comprising using  
11 the error correcting data in the at least some of the packets to correct an error when the  
12 transmitted logical structure is received at the destination.

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14          48. (previously added) The method of claim 43, wherein:  
15           the logical structure includes a header section and a data section; and  
16           the error correcting data is stored in multiple packets in the data section.

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18          49. (previously added) The method of claim 48, wherein information in the  
19 header section of the logical structure indicates what error correcting methodology is used  
20 with the error correcting data stored in the multiple packets in the data section.

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22          50. (previously added) The method of Claim 48, wherein the header section  
23 holds information regarding multiple error correcting methods.

1           51. (previously added) The method of claim 43, wherein the error correcting  
2 data identifies one of a plurality of error correcting methods.

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4           52. (previously added) The method of claim 43, wherein the error correcting  
5 data holds parity bits.

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7           53. (currently amended) In a computer system, a The computer-readable  
8 storage medium as defined in claim 37 holding a logical structure that encapsulates  
9 components comprising:

10           multiple streams of data wherein the streams of data are stored in packets; and  
11           clock licenses that each dictate advancement of a clock that regulates rendering of  
12           the data in the packets, wherein:

13           the streams of data stored in the packets are samples of data from multiple  
14           data streams in packets for transmission on a packet-by-packet basis over a packet  
15           switched network;

16           replicas of information are stored in at least some of the packets;

17           error correcting data is stored in the at least some of the packets;

18           the error correcting data identifies an error correcting method for the at  
19           least some of the packets; and

20           a flag is stored in each said packet that holds the replicas.

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23           54. (previously added) The computer-readable storage medium of claim 53  
24           wherein portions of a sample are stored in selected packets and a replica of property  
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1 information regarding the sample is stored in each packet in which a portion of the  
2 sample is stored.

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4 55. (previously added) The computer-readable storage medium as defined  
5 in claim 53, wherein:

6 the logical structure includes a header section and a data section, and  
7 the error correcting data is stored in multiple packets in the data section.

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9 56. (previously added) The computer-readable storage medium as defined  
10 in claim 55, wherein the information in the header section of the logical structure  
11 indicates what error correcting methodology is used with the error correcting data stored  
12 in the multiple packets in the data section.

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14 57. (previously added) The computer-readable storage medium as defined in  
15 claim 56, wherein the header section holds information regarding multiple error  
16 correcting methods.

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18 58. (previously added) The computer-readable storage medium as defined  
19 in claim 53, wherein the error correcting data identifies a plurality of error correcting  
20 methods.

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22 59. (previously added) The computer-readable storage medium as defined  
23 in claim 53, wherein the error correcting data holds parity bits.

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2 60. (currently amended) A The data processing system as defined in claim  
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4 42 comprising:

5 a source computer with a storage;

6 a logical structure stored in the storage for encapsulating multiple data streams,

7 data from said data streams being incorporated in packets; and

8 a clock license being encapsulated into at least one packet for advancing a clock at

9 a destination when processed at the destination, wherein:

10 the streams of data stored in the packets are samples of data from multiple  
11 data streams in the packets for transmission on a packet-by-packet basis over a  
12 packet switched network;

13 replicas of information are stored in at least some of the packets;

14 error correcting data is stored in the at least some of the packets;

15 the error correcting data identifies an error correcting method for the at  
16 least some of the packets; and

17 a flag is stored in each said packet that holds the replicas.

19 61. (currently amended) A The data processing system as defined in claim  
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21 42 comprising:

22 a source computer with a storage;

23 a logical structure stored in storage for encapsulating multiple data streams, data

24 from said data streams being incorporated in packets; and

1           a clock license being encapsulated into at least one packet for advancing a clock at  
2           a destination when processed at the destination, wherein portions of a sample are stored  
3           in selected packets and a replica of property information regarding the sample is stored in  
4           each packet in which a portion of the sample is stored.

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6           62. (currently amended) The data processing system as defined in claim  
7           6042, wherein:

8           the logical structure includes a header section and a data section, and  
9           the error correcting data is stored in multiple packets in the data section.

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11           63. (previously added) The data processing system as defined in claim 62,  
12           wherein information in the header section of the logical structure indicates what error  
13           correcting methodology is used with the error correcting data stored in the multiple  
14           packets in the data section.

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17           64. (previously added) The data processing system as defined in claim 63,  
18           wherein the header section holds information regarding multiple error correcting  
19           methods.

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21           65. (currently amended) The data processing system as defined in claim  
22           6042, wherein the error correcting data identifies a plurality of error correcting methods.

1           66. (currently amended) The data processing system as defined in claim  
2           6042, wherein the error correcting data holds parity bits.  
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